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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,733	04/14/2004	Choel-Hee Han	P57042	4887

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EXAMINER	
PHAN, THANH S	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,733	HAN, CHOEL-HEE	
	Examiner	Art Unit	
	Thanh S. Phan	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 04/14/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pikula et al. [US 2003/0058742] in view of Myr [US 2002/0183069] and Tursich [US 6,377,517].

Regarding claim 1, Pikula et al. disclose a synchronous time system comprising:

a GPS receiver module [110 and 115] adapted to extract clock information from a received GPS signal, to generate a first clock signal, and to output the first clock signal to a first base transceiver station and a base transceiver station of a next stage [slaves devices 130], and

a clock module [internal clock 420 of slave device; fig 4] adapted to generate a second clock signal [para. [0021]] synchronized with the first clock signal with one of the GPS receiver module of the first base transceiver station or a base transceiver station of a previous stage, and to output the second clock signal to its base transceiver station and a base transceiver station of the next stage upon the clock module receiving a first clock signal from one of the GPS receiver module of the first base transceiver station or the base transceiver station of the previous stage, the clock module being arranged within a base transceiver station other than the first base-station transceiver [para. 19].

Pikula et al. disclose the claimed invention except for explicitly stated wherein the during the propagation process a delay correction is performed and that the time signal components comprises time of day, and the GPS receiver module being arranged within the first base-station transceiver.

Myr disclose a communication system wherein the time of delay is measured [in Timing Block] during the propagation process.

It would have been obvious to one of ordinary skill in the art to incorporate the time of delay measurement design of Myr with Pikula et al. to improve measurement accuracy.

Tursich discloses [figure 1] a structure [140] for synchronizing time comprising a GPS receiver [104] arranged within the structure, and a time of day clock signal [130] within a clock system [102].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the timing structure design as suggested by Turish with Pikula et al. for the purpose of facilitating synchronization of time.

Regarding claim 4, Pikula et al. further disclose wherein the delay correction module is adapted to measure the delay of the clock received in the GPS receiver module of one of the first base transceiver station or the base transceiver station of the previous stage by transmitting the delay correction signal to one of the GPS receiver module of the first base transceiver station or the base transceiver station of the previous stage, and to measure and correct the delay in accordance with a signal returned thereto [para. 21].

Regarding claims 2 and 3, Pikula et al. and Tursich disclose the claimed invention except for a PLL module adapted to generate the first clock signal and first TOD data according to the extracted clock information and TOD information; a driver adapted to output the first clock signal and first TOD data to the first base transceiver station and the base transceiver station of the next stage; a return module adapted to effect delay correction by returning a delay correction signal received from a clock module of the base transceiver station of the next stage.

Myr discloses a communication systems comprising a PLL module [3] adapted to generate signal information; a driver [2] adapted to output signal information to base transceiver stations; a return module [7] adapted to effect delay correction by returning a delay correction signal received.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Myr with Pikula et al., as modified, for the purpose of effective transmitting signal information to accurately synchronize the time signals.

Claims 5, 9 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pikula et al. in view of Myr.

Regarding claims 5, 8 and 9, Pikula et al. disclose a system [100] comprising a main base transceiver station [110] having a GPS receiver module [115] adapted to extract clock information and TOD information from a received GPS signal and to generate a clock signal and TOD data used for operating its base-station transceiver; and at least one sub-base transceiver station [slave devices 130], each at least one

sub-base transceiver station having a clock module [internal clock 420 of slave device; figure 4] adapted to receive a clock signal and TOD data from one of the GPS receiver module of the main base transceiver station or an adjacent base transceiver station through a daisy chain, and to generate a clock signal and TOD data synchronized with the clock signal and the TOD data used in the main base transceiver station with one of the GPS receiver module which has transmitted the clock signal and the TOD data or the adjacent base-station transceiver [para. 19- para. 21]. Since Pikula et al disclose wherein more than one slave devices are in the system; therefore, the limitations of claim 9 are disclosed.

Pikula et al. disclose the claimed invention except for explicitly stated wherein the during the propagation process a delay correction is performed.

Myr disclose a communication system wherein the time of delay is measured [in Timing Block 7] during the propagation process.

It would have been obvious to one of ordinary skill in the art to incorporate the time of delay measurement design of Myr with Pikula et al. to improve measurement accuracy.

Regarding claims 6 and 7, the method steps are necessitated by the apparatus structures as disclosed by Pikula et al and Myr, wherein a system is capable of extracting clock information and TOD information from a received GPS signal, with a first base transceiver station having a GPS receiver module; outputting a clock signal and TOD data used for operating the first base transceiver station from the extracted clock information and TOD information from the first base-station transceiver; receiving

clock signals and TOD data from one of the first base transceiver station or abase transceiver station of the previous stage through a daisy chain, with abase transceiver station other than the first base-station transceiver; measuring and correcting delays of the received clock signals and TOD data with a base transceiver station other than the first base-station transceiver; and generating clock signals and TOD data synchronized with the clock signal and the TOD data used in the first base transceiver station by reflecting a value of the delay correction to the received clock signals and TOD data, and outputting the synchronized clock signals and TOD data to its base transceiver station and the base transceiver station of the next stage, with a base transceiver station other than the first base-station transceiver; wherein measuring and correcting the delay includes transmitting the delay correction signal to one of the first base transceiver station or the base transceiver station of the previous stage, and measuring and correcting a delay using a signal being returned, in order to measure a clock delay received from one of the first base transceiver station or the base transceiver station of the previous stage.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Weedon et al. [US 2003/0156498] ; Mitsugi [US 6,959,198] ; Ishigaki [US 6,563,765] ; Kihara et al. [US 6,298,014].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh S. Phan whose telephone number is 571-272-2109. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

tsp